UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,300	12/28/2001	Hong Suk Yoo	8733.508.00-US	2980

30827 7590 12/06/2005

MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
DUONG, THOI V	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 12/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,300	YOO ET AL.	
	Examiner	Art Unit	
	Thoi V. Duong	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7,9,11-14 and 17-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6 and 17-31* is/are allowed.

6)☒ Claim(s) *1,2,7 and 11-14* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 02, 2005 has been entered.

Accordingly, claims 1 and 7 were amended, and claims 3, 4, 8, 10, 15 and 16 were cancelled. Currently, claims 1, 2, 5-7, 9, 11-14 and 17-31 are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawahata (USPN 6,356,318 B1).

Re claim 1, as shown in Figs. 1 and 2, Kawahata discloses a liquid crystal display device including a data line 13 supplied with a data signal, a gate line 7, 7' supplied with a scanning signal, a pixel electrode 19 for driving a liquid crystal cell, and a thin film transistor 11 for applying the data signal to the pixel electrode in response to the scanning signal, the device comprising:

a gate insulating film comprising a superposed gate insulating film 8 and an insulating film 10 (col. 4, lines 45-47) entirely covering the gate line 7, 7' wherein the data line 13 is disposed on the gate insulating film 8, 10; and

a storage electrode 15 sunken in the gate insulating film 8 to overlap with the gate line 7', said storage electrode 15 uncovered by and disposed on said gate insulating film 10; and

a protective layer 16 on the gate insulating film 8, 10 to cover the data line 13, the gate line 7, 7' and the thin film transistor 11,

wherein a contact hole 9 passes through the protective layer 212 and a portion of the gate insulating film 8 having the storage electrode 15 formed therein and wherein the pixel electrode 19 is connected to the storage electrode 15 via the contact hole 9.

Re claim 2, Kawahata discloses that the thickness of the insulating film 10 is in the range of 500 to 1500 angstroms; therefore, the distance between the gate line 7'

and the storage electrode 15 is also the thickness of the insulating film which is in the range of 500 to 1500 angstroms.

4. Claims 1, 2, 7 and 11-14 rejected under 35 U.S.C. 102(e) as being anticipated by Jung et al. (Jung, USPN 6,317,173 B1).

Re claim 1, as shown in Figs. 50 and 51, Jung discloses a liquid crystal display device including a data line 600 supplied with a data signal, a gate line 401 supplied with a scanning signal, a pixel electrode 800 for driving a liquid crystal cell, and a thin film transistor for applying the data signal to the pixel electrode in response to the scanning signal, the device comprising:

a gate insulating film comprising the insulating films 54 and 500 entirely covering the gate line 401, wherein the data line 600 is disposed on the gate insulating film 500; and

a storage electrode 64 sunken in the gate insulating film 500 to overlap with the gate line 401, said storage electrode 64 uncovered by said gate insulating film 500 and disposed on the gate insulating film 54 (col. 22, lines 42-56); and

a protective layer 700 on the gate insulating film 54, 500 to cover the data line 600, the gate line 401 and the thin film transistor,

wherein a contact hole C16 passes through the protective layer 700 and a portion of the gate insulating film 500 having the storage electrode 64 formed therein and wherein the pixel electrode 800 is connected to the storage electrode 64 via the contact hole C16 (Fig. 51).

Re claim 2, since the thickness of the insulating film 50(54) is 500 angstrom-3000 angstrom, a distance between the gate line 401 and the storage electrode is also about 500 angstrom-3000 angstrom (col. 23, lines 1-4)

Re claim 7, as shown in Figs. 50 and 51, Jung discloses a liquid crystal display (LCD) device comprising:

a gate line 401 and a data line 600 on a substrate 100 to cross each other;

a thin film transistor including a gate electrode 410, a source electrode 610, and a drain electrode 620, and provided at an intersection between the data line and the gate line;

a storage electrode 64 on a first gate insulating film 54(50) to cover the gate electrode 410 and the gate line 401 (see also Fig. 52C; col. 22, lines 41-49);

a second gate insulating film 500 formed on the first gate insulating film 54 wherein the data line 600 is disposed on the second gate insulating film 500 so that the gate line 401 is electrically isolated from the data line 600; and

a protective layer 700 formed on the second gate insulating film 500 to cover the gate line 401, the data line 600 and the thin film transistor,

wherein a first contact hole C16 passes through the protective layer 700 and a portion of the second gate insulating film 500 having the storage electrode 64 formed on the first gate insulating film 54, wherein the storage electrode 64 is connected to a transparent electrode pattern 800 via the first contact hole C16 (col. 21 line 66 through col. 22, line 4) and wherein a storage capacitor includes the storage electrode 64 and

the gate line 401 opposed to each other and having the first gate insulating film 44 formed therebetween (col. 22, lines 42-54); and

wherein, re claim 14, a pixel electrode 800 is connected to the drain electrode 620 via a second contact hole C3 provided on the protective layer 700 (Fig. 51);

Re claim 11, the gate electrode 410 is connected to the gate line 401 (Fig. 50).

Re claim 12, the source electrode 610 is connected to the data line 600 (Fig. 50).

Re claim 13, the drain electrode 610 is opposed to the source electrode 620, and wherein a channel 220 is formed between the source electrode and the drain electrode.

Response to Arguments

5. Applicant's arguments filed September 02, 2005 have been fully considered but they are not persuasive.

Re claim 7, Applicant argued that nothing in Jung teaches or suggests "a storage electrode on a first gate insulating film to cover the gate electrode and the gate line"; in contrast, Jung teaches a separate "insulating film for a storage capacitor formed on the first storage electrode." The Examiner disagrees since the insulating film 54 covering the first storage electrode 440, which is a part of the gate line 401 (col. 22, lines 41-45), and the insulating film 51 covering the gate electrode 410 are patterned from the same gate insulating film 50 (col. 23, lines 1-14); and the second storage electrode 64 is formed on the insulating film 54 as shown in Figs. 50, 51 and 52C of Jung. Thus, Jung teaches or suggests "a storage electrode on a first gate insulating film to cover the gate electrode and the gate line."

Allowable Subject Matter

6. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. See below reasons for allowance.

7. Claims 5, 6 and 17-31 were previously allowed.

The following is an examiner's statement of reasons for allowance: none of the prior art of record fairly suggests or shows all of the limitations as claimed. Specifically,

Re claims 5 and 17, none of the prior art of record discloses, in combination with other limitations as claimed, a storage electrode formed on a first gate insulating film to overlap with the gate line, a second gate insulating film deposited on the first gate insulating film to cover the storage electrode, an active layer and an ohmic contact layer formed on the gate insulating films, a source electrode and a drain electrode on the ohmic contact layer, a protective layer on the gate insulating films to cover the source electrode and the drain electrode, and a pixel electrode connected to the drain electrode and the storage electrode on the protective layer.

The most relevant references, USPN 6,356,318 B1 to Kawahata and USPN 5,998,838 to Tanabe et al. (Tanabe), fail to disclose or suggest the claimed invention.

As shown in Fig. 1, Kawahata discloses a first gate insulating film 8 and a second gate insulating 10 deposited on the first gate insulating 8; however, the storage electrode 15 is formed on top of the second gate insulating layer 10. Meanwhile, as shown in Fig. 11 (c), Tanabe only discloses an active layer 1015 and an ohmic contact

layer 1017 formed on a second gate insulating film 1014b to overlap with a gate electrode 1013a.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thoi V. Duong whose telephone number is (571) 272-2292. The examiner can normally be reached on Monday-Friday from 8:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached at (571) 272-2293.

Thoi Duong

11/30/2005

ANDREW SCHECHTER
PRIMARY EXAMINER